APPLICATION NOTE AN110

SL3522 Applications and Characteristic Data

Supersedes April 1994 version, AN110-2.0

AN110-3.0

This application note provides information to assist users to achieve the full performance from the SL3522 in their chosen applications.

PRODUCT DESCRIPTION

The SL3522 is a complete monolithic successive detection Log/Limiting amplifier which can operate over an input frequency range of 100MHz to 500MHz. Producing a Log/Lin characteristic for signals between −64dBm to +6dBm; the log amplifier can provide an accuracy of ±1dB.

It consists of 6 gain stages, 7 detector stages, a limiting RF OUTPUT buffer and VIDEO OUTPUT amplifier. The power supply connections to each section are isolated from each other to aid stability. Each of the gain stages and detector stages has approximately 12dB of gain, and a significant amount of on-chip RF decoupling also to aid stability.

The limiting RF OUTPUT buffer provides a balanced limited output level of 0dBm on each RF OUTPUT line (pins 9 and 10), for input signal levels in excess of −65dBm (when input applied to pins 27 and 28). It can be isolated from the other parts of the log/limiting amplifier, by disconnecting the RF OUTPUT Buffer GND (pin 8) from 0V. This feature will aid stability in applications which do not require a limited RF OUTPUT.

The video amplifier provides a positive-going output signal proportional to the log of the amplitude of an RF INPUT applied to pins 27 and 28, the gain and offset of the video amplifier can be adjusted by means of 3 resistors, R_G, R_T and R_O which are connected to the Gain Adjust pin (19), Trim Ref (pin 18) and Offset Adjust (pin 17) respectively. With R_T set to 1.5kΩ, R_G can be set to any value between 1kΩ and achieve a range in offset between −0.5V and +1.0V.

The RF INPUT pins (pins 27 and 18) have a 50Ω terminating resistor connected between them on-chip. These in turn are capacitively coupled to the input gain stage. The RF INPUT has provision to be driven either balanced or single ended.

The SL3522 consumes approximately 1·1 watts of power when all parts of the circuit are powered up from a ±5.0V power supply. As the circuit uses a class A based differential architecture the power consumption of the RF gain stages, detectors and RF OUTPUT buffers will be independent of input signal level. However, the VIDEO OUTPUT (pin 13) is single ended, and the power consumption of the video amplifier will vary with RF INPUT signal level on pins 27 and 28.

If the SL3522 is operated with the RF OUTPUT buffer disabled (i.e. RF OUTPUT buffer GND, pin 8, left floating), the power consumption will drop to approximately 0.95W, when all other parts of the circuit are powered from a 65.0V power supply.

RF OUTPUT Buffer

The SL3522 contains 70dB of broadband RF gain with 3dB bandwidth of 450MHz. When the RF OUTPUT buffer is powered up, this gain can be realised at the RF OUTPUT ± pins (9 and 10). Operating the device with the RF OUTPUT buffer powered down removes the RF OUTPUT and results in a Log Amplifier with enhanced stability and reduced power consumption.

The RF OUTPUT GND pin (8) is the positive supply to the RF OUTPUT buffer. If this pin is left open circuit the RF OUTPUT amplifier powers down and saves 30mA power consumption from the V_{EE} supply.

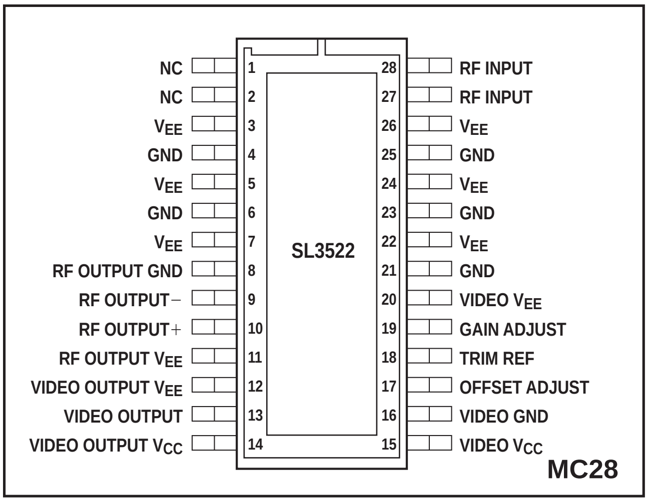

Fig. 1 Pin connections (top view)

The RF OUTPUT V_{EE} pin (11) should always be connected to the V_{EE} supply rail even if the RF OUTPUT buffer is powered down, by operating with pin 8 left open circuit.

If the RF OUTPUT buffer is to be used, care is required in layout to ensure stability.

Application Suggestions

The following precautions should be observed when configuring the device for application:

(a) The device should be mounted on a ground plane, and all supply decoupling should be RF quality chip capacitors. The leads to the decoupling capacitors should be kept as short as possible.

(b) The RF V_{EE} pins (3, 5, 7, 20, 22, 24 and 26) should be connected to a low impedance copper plane. A two layer PCB should help to achieve this.

(c) The load current at the VIDEO OUTPUT pin should be returned to the VIDEO OUTPUT V_{CC} pin (14) via a 10nF capacitor connected to the return line of the video load, avoiding any common impedance path.

(d) The VIDEO OUTPUT V_{EE} pin (12) should be decoupled directly to the VIDEO OUTPUT V_{CC} pin (14) with a 10nF capacitor.

(e) The unscreened lead length at the RF INPUT should be kept to a bare minimum. If being driven single ended, the RF INPUT return line should be isolated from, but kept in very close proximity to the ground plane and connected to the ground plane via a 50Ω chip or bead resistor at pin 18. The RF INPUT can also be driven differentially.

(f) If the device is operated with the RF OUTPUT buffer powered up then care must be taken to present both the RF OUTPUT− (pin 9) and RF OUTPUT+ (pin 10) with matched loads. Each pin should ideally be loaded with a 50Ω terminated transmission line. The device stability is very sensitive to imbalance at the output.

Driving highly reactive SWR loads is not recommended for stability reasons.
(g) Although the RF OUTPUT ± (pins 10 and 9) have DC blocking capacitors shown, they may be operated with a DC load to ground. However, a DC offset of approximately −400mV will exist on each RF OUTPUT pin. It will NOT be possible to power-down the output buffer under these conditions.
(h) The RF INPUT is isolated from the input amplifier by two series on-chip capacitors. The device includes an on-chip 50Ω termination resistor which is connected directly across the RF INPUT pins (27 and 28).

Gain and Offset Trimming

Gain and offset trimming are unilaterally independent. Adjustment of gain has an effect on the offset, but adjustment of offset does not affect the gain.

The gain and offset control is achieved by adjusting R_G and R_O respectively. The control is dependent upon their difference from the trim reference resistor R_T. Differing temperature coefficients in all of these resistors will lead to variations in gain and offset over the temperature range. It is recommended that resistors of identical type be used, to maintain operating stability over temperature.

Video Performance

In order to achieve the specified transient performance, it is important to ensure that the resistor connected to the trim reference pin (18), has a parasitic capacitance less than 5pF. This resistor should have a nominal value of 1·5kΩ. Additionally, the load must be not less than 200Ω resistive with not more than 20pF of shunt capacitance.

Because of the difficulty in making a valid fall time measurement, this parameter is unspecified. It is that time corresponding to a 30mHz bandwidth system incorporating critical damping.

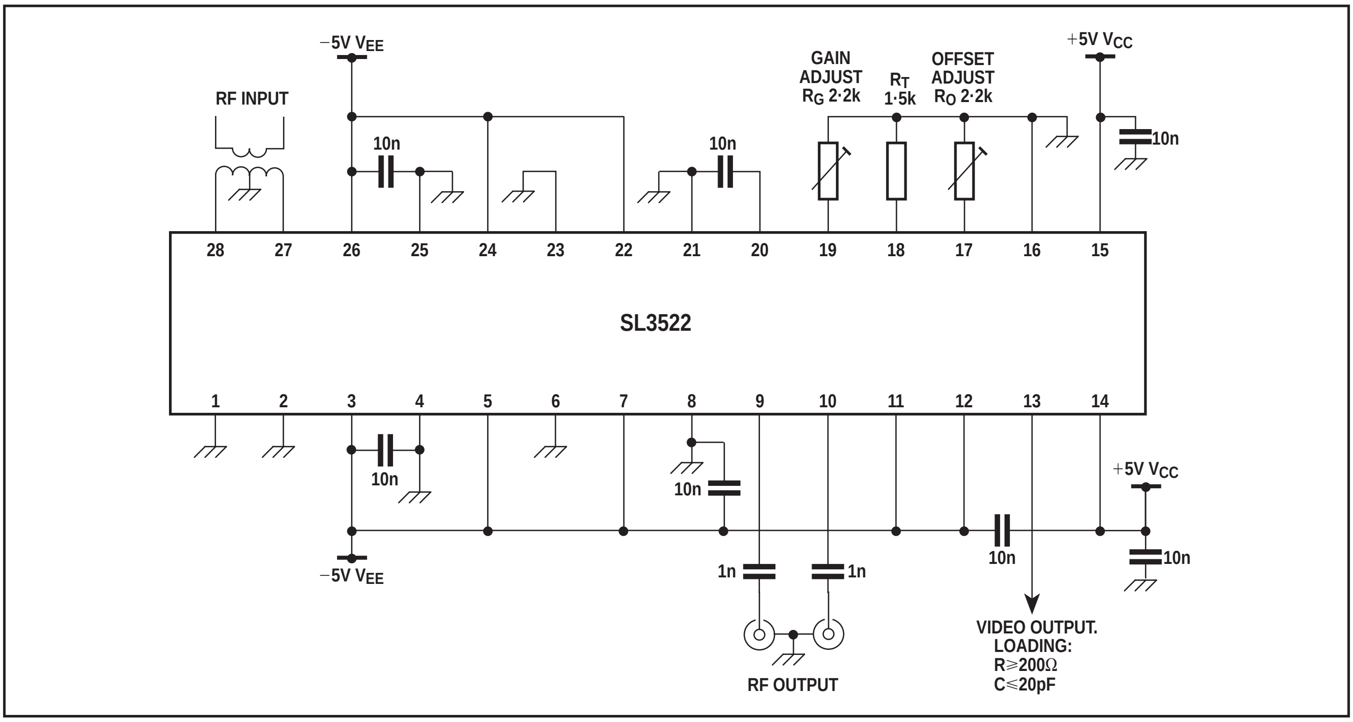

Fig. 2 Test and application circuit

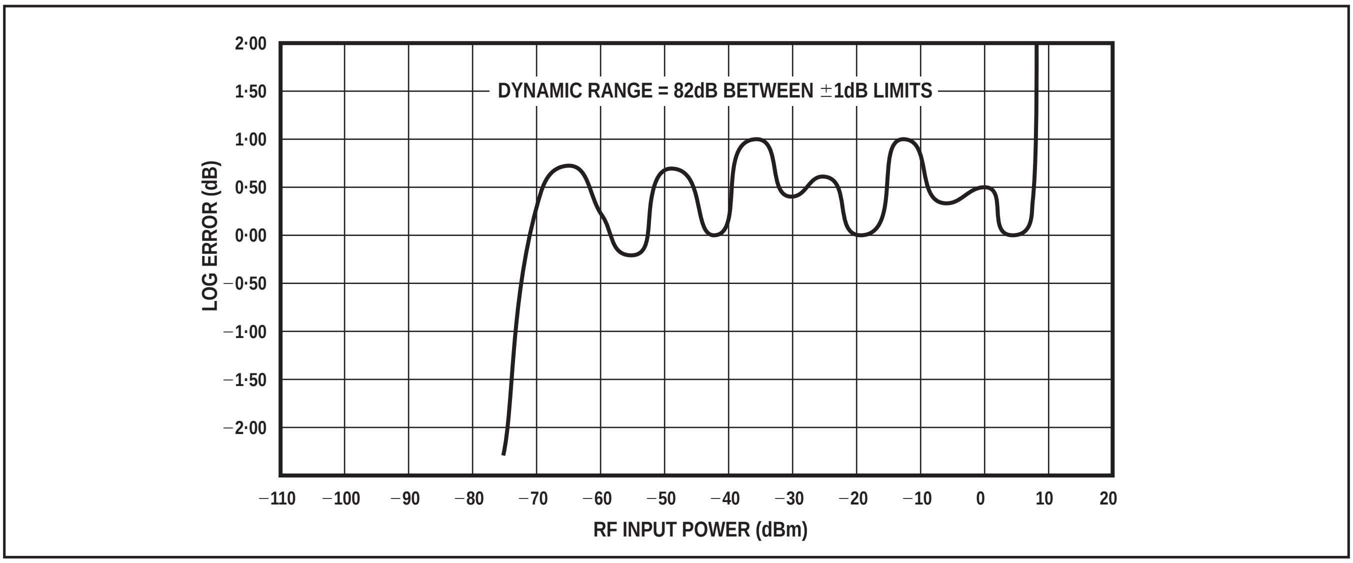

Fig. 3 Typical differential log/lin characteristic

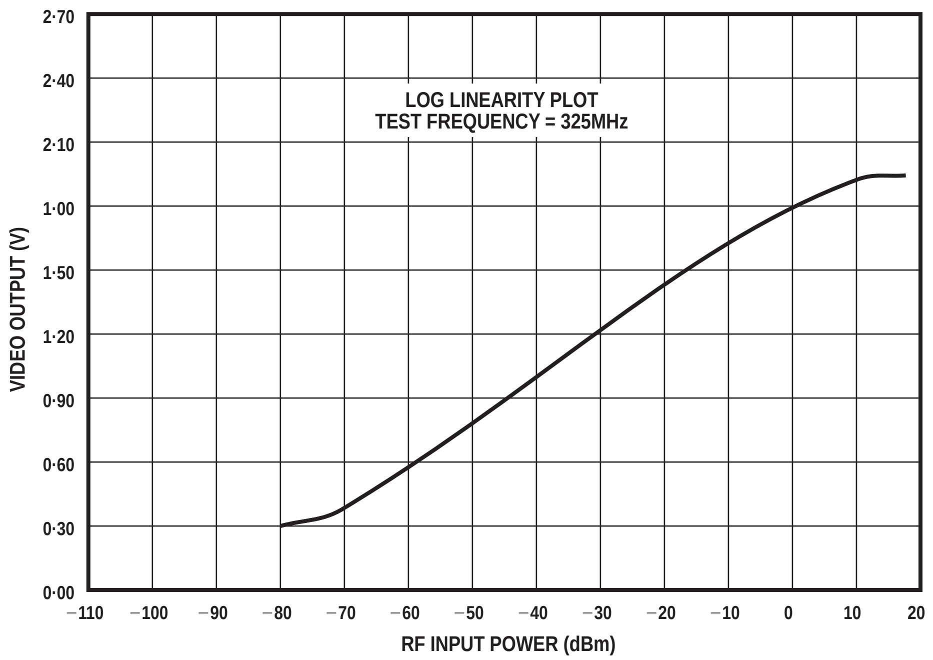

Fig. 4 Typical log/lin characteristic

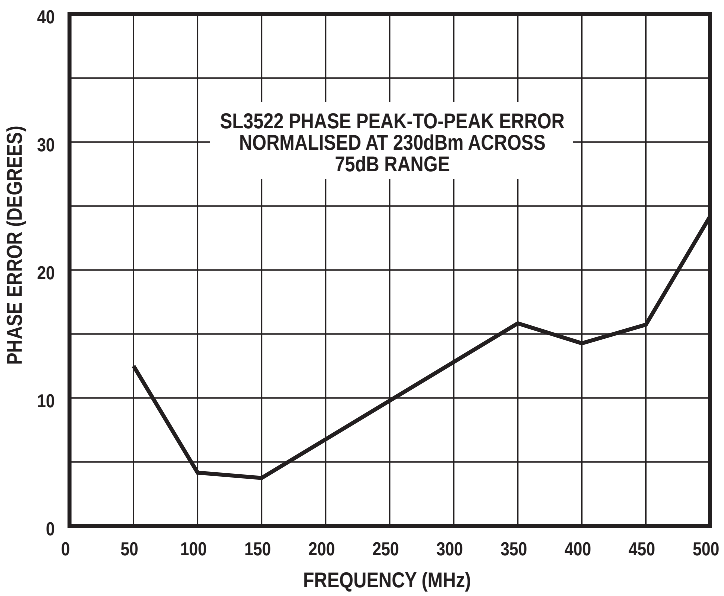

Fig. 5 Typical peak-peak phase variation v. IF frequency with input power between −65dBm and +10dBm, normalised to phase at −30dBm

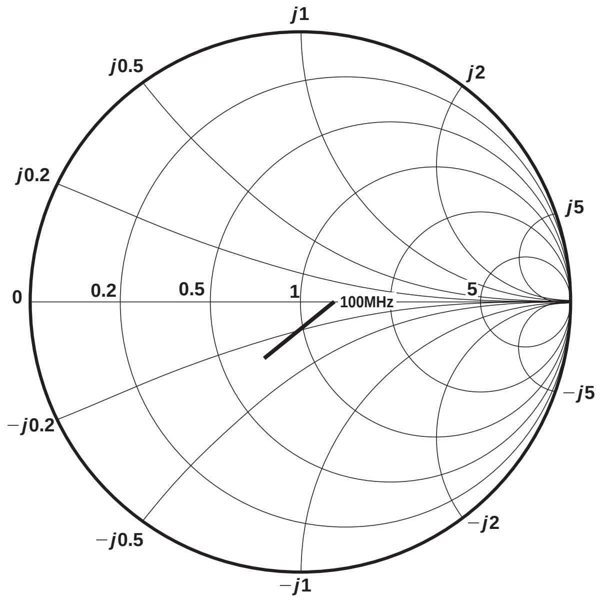

Fig. 6 Typical input impedance normalised to 50Ω. −20dBm input level.

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